MXR-113 Circuit description and troubleshooting tips   R. Grieb tauntek.com

Updated 6/09/2024 to reflect some information provided by designer Tony Gambacurta.

First I should mention that I never worked at MXR and had nothing to do with the design of the MXR-113. I am trying to help people who are interested in repairing their units to understand how it works. This is a somewhat complex design, so there may be mistakes in this document. Since I have no way to draw lines over signal names in this document, I will indicate active-low signals with a lower case b at the end.

Since the MXR-113 contains quite a bit of digital circuitry, you will need an oscilloscope to find all but the simplest problems. Many of the IC's are not socketed, so a shotgun approach is not really workable here. Also, many of them are older 74xx types that are not readily available. If you don't have an oscilloscope, and you expect to work on more units of this complexity, consider getting an inexpensive used one. 50 MHz or larger bandwidth should be fine. You want at least two channels. Scopes like this can often be bought for $50-100.

The schematics for the MXR-113 are available on the web, so you should download them and look over the different sections.

The first step is always a visual inspection, to check for any signs of damage, either from overheating, or possibly a poorly or incorrectly executed previous repair. Something that has been dropped can have a cracked circuit board, with many traces broken along the crack. Solder joints on some components such as large capacitors, or the leads of potentiometers or switches, can crack and no longer connect the lead to the circuit board.

The next thing to check on many repairs would be the power supply voltages. The 113 uses 7 of them. Many devices from this time period used tantalum filter capacitors and these sometimes fail and become a short to ground. A simple DMM is all you need to verify that the supply voltages are correct. Zener diodes may have a voltage tolerance of 5%, so don't expect the voltage to match the value shown exactly. Three-terminal regulators are usually within a few tenths of a volt, in my experience.

If the supply voltages look OK, I suggest feeding a sine-wave into the device and monitoring it with a scope as it passes through the circuit. A triangle wave or sawtooth could be used if no sine wave generator is available.

The 113 mother board schematic shows how the signal flows through the device. If possible, place the unit so that the bottom of the mother board can be probed, as this should allow tracing the audio signal through the circuit. Once the problem has been isolated to a particular board, then you can try to probe the chips on that board.

The input passes through diff amp A11-5,6,7 and variable-gain amp A11-1,2,3 and then is fed to the input low-pass filter at J4-5. The input filter consists of three cascaded low-pass stages. The cutoff frequency can be set to one of four values, by the signals at pins 1 and 2 of J4. The output of the input filter is at J4-6. Using a 'scope you should see the input signal feeding into J4-5 and coming out of J4-6 (having been low-pass filtered)

The signal is now fed into a compressor circuit on the compander board, at J5-6.

The compressor has a non-linear response. Signals with higher amplitude are amplified less than weaker ones. Compressing the signal allows fewer bits to be used to store it later on. You should see the signal coming into the compressor at J5-6 and exiting at J5-7. If you vary the level of the signal and watch the input and output at the same time, you should be able to observer the compressor action. The data sheet for the NE571 chip will help to understand exactly how the compressor circuit works.

The output of the compressor feeds into J7-10 on the switching board. It is sampled by analog switch SC1-1,2,13 with the voltage sample saved on C6. This voltage feeds through unity-gain buffer A5 and into one input of A7 "error amp". The other input to the error amp is the output of a D->A convertor made up of Q5,3,4,6 and associated diodes and resistors. So the error amp output is related to the difference between the DAC output and the voltage sample at C6. The output of the error amp can be selected as the input to comparator A8 using SC2-1,2,13. The output of A8 is fed to the TTL board at J7-6.

It should be possible to feed a constant voltage and frequency waveform into the 113 and follow it through the input amps, the input filter, the compressor, and see it at J7-10. That would confirm that it's making it to the input to the analog->digital converter.

Digital fun:

The MXR converts analog samples of the input signal to digital values, stores them in a RAM buffer, then retrieves them later, converts them back to analog, expands them, filters them, and sends them out.

The following text relates mostly to circuits on the TTL board.

Digital circuits use a clock signal to pace their operation. The frequency of this clock is much higher than the frequency of the analog signals being processed. Often this main clock is generated by a crystal oscillator, but sometimes it needs to be varied, so a different method is used. In the 113, the 74LS221 called SC1 is used to generate the main digital clock. This chip contains two pulse generators, and each one is set up to trigger the other when it times out, so they keep going forever. The pulse width of both can be varied by the voltage at J6-14. When it is made narrower, the oscillator frequency is increased. The main clock signal can be seen at A5-8 and should be a stable clock (when the sweep fcn is not being used).

Since the main clock signal is used to pace the operation of the digital logic, which controls sampling the input, writing it to RAM, and then reading it out again, if we make the clock run slower, all of that happens at a slower pace, which increases the delay value. So the main clock can be varied to change the delay, and this is what the sweep circuit does. The front panel Delay control also varies the clock frequency over a 4:1 range. On my test unit, with sweep disabled, the clock at A8 pin 8 could be varied from about 1.4 MHz to about 5.6 MHz.

A14 and A7 are a programmable divider of the master clock.
Check A13-12 for a clock signal, and also pins 8 and 9.

A6 is a counter. Pins 11,9,and 8 count from 0-7 and pin 12 toggles after each 0-7 cycle.

A4 is a decoder. One output pin of this chip should pulse low at a time, in sequence, over and over: 1,2,3,4,5,6,7. These outputs operate a successive-approximation circuit composed of A5, Q1, A13, A12, A11. They also control input sampling, reading and writing to DRAM and when the DRAM address increments.

The switching board A8 comparator output signal is fed to the base of Q1. As we saw above, this comparator can compare the DAC output to a voltage sample of the input waveform. So the comparator can tell us if the DAC voltage is higher or lower than the sample. The value at TTL board Q1 is written into the A13, A12, and A11 flip flops in sequence by the strobes from A4, (via A5) to form the digital equivalent of the analog sample being converted. (In some other designs, the fcns of A6,A4,A5,A13,A12, and A11 would all be performed by a single chip.) Analog to digital conversion of the input sample is performed in two 0-7 cycles of counter A6 pins 9,8, and 11. The first cycle creates a 5-bit value that is roughly equivalent to the input sample. During the second cycle, this value is fed to the DAC and the DAC output is compared to the input sample. The error is then multiplied by a factor of 32 and converted into a second 5-bit value. Both values are stored in RAM. The first value represents the 5 most significant bits of the 10-bit equivalent of the input sample, and the second value corresponds to the 5 least significant bits.

Gates A19, A18, and A20 form a 5-bit 2:1 multiplexor, which can either feed the output of the successive approximation circuit to the DAC (used when we are converting a sample to digital) or the output of the RAM buffer (used when we are playing back a sample) via register chip A17. So the same DAC is used for both functions, and is constantly switching back and forth between them.

After the successive-approximation circuit has arrived at the digital values which matches the sample voltage, those two 5-bit values are written to the DRAM memory buffer chips.

Binary counter chips A15, A1, and A16 generate the 12-bit address needed by a 4K-word DRAM buffer. But there are four 4K-word memory boards, so we need to select one of these to be active at a time. Multiplexer A8 selects one of the 8 upper bits of the address counter to feed into A9-2. This determines the number of addresses that we count through before we either start over in the same memory board, or switch to the next board (more on that in a bit) So this determines the size of the buffer, which determines the amount of delay. and we can see that the select inputs to A8 come from the front-panel delay range switches. The output of A8 is fed to A9-2 and then to A2-9. A2-10 output is called "board select pulse" and feeds to J1-20. On the mother board schematic, we can see that this pulse is used to clock two flip flops (A4) to form a 2-bit counter. The outputs of this counter are decoded by A5 to form four "board selects", only one of which is active at a time.

Since we only have one address counter, and one board select signal active at a time, it seems that we must write to and read from the same address. So probably we read one 5-bit part of the sample from that address, and then write five bits of the new value into that same address. Two memory refresh cycles are performed in-between each of the read-then-write cycles mentioned above. This is necessary to satisfy the refresh requirements of the DRAM chips.

But using A8, we can vary the length of our buffer to select a delay range, and then within that range, we can vary the delay by varying the master clock frequency using Q2,Q3 on the TTL board.

On the mother board schematic, we can see that the PRESETb input to flip flops A4 is fed to J11. This signal can be fed to +5V (no preset) or CS2b, CS3b, or CS4b. This is a jumper setting which needs to match the number of memory boards installed. If only one board is installed, it must be in slot J2, and the jumper would select signal CS2b. This would reset the A4 flip flops as soon as CS2b goes active, forcing the first memory board to always be selected. Connecting the jumper to CS3b would alternate between memory boards J2 and J3. So for troubleshooting, it may be useful to set the jumper to only enable the use of J2. This will allow testing each memory board individually in slot J2. The delay will be shorter, of course, in this mode.

Once the sample has been read from the buffer, it is converted back to analog form, and sampled at pin 3 of A2 on the switching board. From there it passes through A3 and is again sampled by C8 and buffered by A4. The output is fed to J7-11, and routed to J3-8. This is the input to the expander part of the compander board. The output of the expander is at J3-9, and is fed to J4-8, the input of the Output low-pass filter. The output of the filter is at J3-9. This signal is fed through a circuit (A10 on the motherboard) that either passes it unchanged or inverts it. The output at A10-1 is fed into the mix control where it can be mixed with the input to the 113, then through bypass/normal analog switch A8, level control amplifier A9, and to the output jack.

One thing I noticed: The MXR documentation implies that the signal out will be at the same level as the input signal. The input amplifier A11 pins 5,6,7 can be fed with a differential (balanced) input or a single-ended one. If a balanced input is used, the gain of this stage will be twice what a single-ended input will get, since the single-ended input only connects to one of the two inputs to this stage. It seems that if a single-ended input is used, the output signal level will be half of the input signal level.

Each sample is either read or stored in 16 cycles of the clock at A5-8. If four memory boards are installed, we have a total of 16,384 5-bit words or 8,192 samples of storage. If that corresponds to 640 mSec of delay, then the time between samples should be 640 mSec/8192 or 78.1 uSec. A14 has outputs which divide the main clock by 2,4,8,or 16. To get the maximum delay, we would divide by 16. In that case, 78.1 uSec is 256 cycles of the main clock, so the clock would be 3.28 MHz. 640 mSec is the value with the front panel delay control set to the middle, so the maximum delay should be 3.28/2 or 1.64 MHz, and minimum delay freq would be 6.56 MHz. The clock freq on my test unit was a little lower than this and I noticed that the delays were a little longer than expected, so probably it needs adjustment.

As mentioned above, two DRAM addresses are skipped in-between successive read/write operations. But we want to use all of the DRAM addresses to get the maximum delay. Since every third address is used, we end up using every address. Consider the sequence in the case where the DRAM has only 8 addresses:

Read/Write 0
skip 1
skip 2
R/W 3
skip 4
skip 5
R/W 6
skip 7
skip 0 (address wraps)
R/W 1
skip 2
skip 3
R/W 4
etc.

Because 8 (or 4096) is not a multiple of 3, we use different addresses each time through the DRAM and end up using every one.

Motherboard trimmers:

My test unit only seemed to have two MB trimmers. The one next to the two vertical 100 uF caps is used to adjust the +15V supply to have the same value as the -15V supply.

The other trimmer, closer to "Board Select", was the one shown as R42 on the schematic. This adjusts the frequency of the main clock.   In my case, I have four memory boards installed, so if I monitor CS3, select "640 mSec" and set the Delay control to maximum, I can set the trimpot so that CS3 repeats every 1280 mSec.   (640 is the center value, not the maximum)

Anyway, I hope this document will be of use to someone working on an MXR-113.