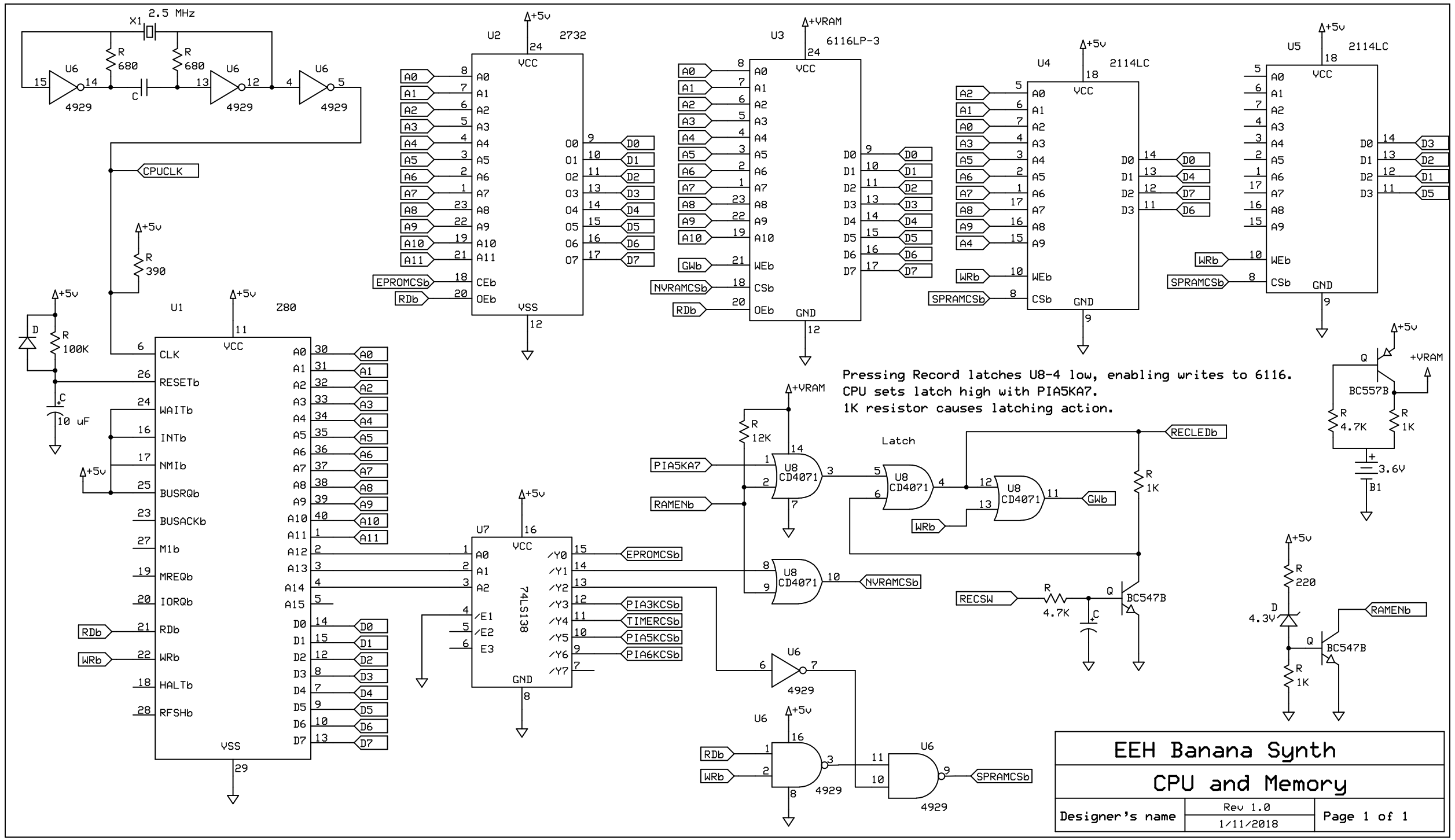
X1 2.5 MHz
U6 4929
R 680
C
CPUCLK
+5v
R 390
D
R 100K
C 10 uF
U1 Z80
CLK
RESETb
WAITb
INTb
NMIb
BUSRQb
BUSACKb
M1b
MREQb
IORQb
RDb
WRb
HALTb
RFSHb
VCC
VSS
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15
D0 D1 D2 D3 D4 D5 D6 D7
U2 2732
EPROMCSb
U3 6116LP-3
GWb
NVRAMCSb
+VRAM
U4 2114LC
SPRAMCSb
U5 2114LC
U7 74LS138
/Y0 /Y1 /Y2 /Y3 /Y4 /Y5 /Y6 /Y7
/E1 /E2 E3
PIA3KCSb
TIMERCSb
PIA5KCSb
PIA6KCSb
R 12K
PIA5KA7
RAMENb
U8 CD4071
Latch
RECLEDb
R 1K
RECSW
R 4.7K
Q BC547B
Q BC557B
R 4.7K
R 1K
3.6V
B1
R 220
D 4.3V
Pressing Record latches U8-4 low, enabling writes to 6116.
CPU sets latch high with PIA5KA7.
1K resistor causes latching action.
EEH Banana Synth
CPU and Memory
Designer's name
Rev 1.0
1/11/2018
Page 1 of 1